LANA Example 2: Algorithm Implementation

on a Circuit with 8 Resistors, 2 Voltage Sources, 2 Current Sources

Example 2: Ideal schematic diagram

In this document, we use the Linear-Algebraic Nodal Analysis (LANA) algorithm to analyze an electric circuit that includes eight $1k\Omega$ resistors, two 5V dc voltage sources, and two 2.5mA dc current sources. Figure 1 is an ideal circuit diagram that provides a complete description of this circuit.



Figure 1: An ideal schematic diagram of a circuit containing eight resistors, two dc voltage sources, and two dc current sources.

To run the LANA algorithm, we follow the seven steps as outlined in either the Quick reference guide or the Step-by-step guide to the LANA algorithm. The title of each (sub)section in this document corresponds to a unique (sub)step in the LANA algorithm. In this work, we share entry-by-entry definitions for many of the matrices and equations used to model the circuit given in Figure 1. The goal of this effort is to help the reader check their work while becoming more familiar with both the block-matrix and entry-by-entry definitions used in this algorithm.

Step 1: Identify and label all circuit nodes

We start our work in the LANA algorithm by explicitly identifying and enumerating the individual nodes of our ideal circuit. To do so, we use the *node identification heuristic* in which we erase the bodies of all ideal circuit elements and leave only the leads. The remaining, contiguous segments of conductor are known as the *nodes* of the circuit. In Figure 2 below, we redraw our ideal circuit schematic diagram from Figure 1 using this node identification heuristic. We then count and enumerate the nodes of this circuit using positive integers. In this example, we see our circuit has seven nodes.



Figure 2: The skeleton circuit of contiguous wire segments that results from the node identification heuristic applied to the circuit from Figure 1. Notice the body of each circuit element is replaced with a blank space.

Step 2: Model the circuit using a directed graph

The second step in the LANA algorithm is to represent the topology of our circuit as a directed graph $\mathcal{G} = (\mathcal{N}, \mathcal{E})$. We should check that we have a complete description of a circuit that contains only resistors, dc voltage sources, and dc current sources. The circuit presented in Figure 1 meets these specifications.

Step 2A: Track the dimensions of key features in our circuit

The nodes of our digraph correspond to the circuit nodes and represent the interconnections between the circuit elements. For this specific example, we see the set of digraph nodes is given as

$$\mathcal{N} = \{1, 2, 3, 4, 5, 6, 7\}.$$

The positive integer $n_g \in \mathbb{N}$ denotes the number of elements in set \mathcal{N} . In this example, $n_g = 7$ since we identified and enumerated 7 nodes in step 1 of the algorithm.

Next, we replace each circuit element with a directed edge in our digraph model. We write each edge $e \in \mathcal{E}$ as an ordered pair of nodes with $\mathcal{E} \subset \mathcal{N} \times \mathcal{N}$. The direction of edge e = (2, 1) goes from node 2 to node 1. In other words, we say that edge e = (2, 1) leaves node 2 and enters node 1.

The variable $m \in \mathbb{N}$ represents the total number of edges in our graph. Because each edge of our digraph corresponds to a single circuit element, the number of edges equals the number of circuit elements. To count the edges, we sum of the number of resistors, denoted as $m_r \in \mathbb{N}$, the number of dc voltage sources, denoted as a nonnegative integer $m_v \in \mathbb{Z}$, and the number of dc current sources, denoted as a nonnegative integer $m_i \in \mathbb{Z}$. Mathematically, we write

$$m = m_r + m_v + m_i.$$

As we see in Figure 1, there are a total of $m_r = 8$ resistors, $m_v = 2$ dc voltage sources, and $m_i = 2$ current sources. Accordingly, our directed graph model of this circuit has m = 12 edges.

Step 2B: Orient and enumerate the edges of the digraph

We choose the direction of each edge in our digraph using some knowledge of electronics. Specifically, we orient each edge associated with a dc current source in the same direction as the current flow provided by that source. The reference direction of each edge corresponding to a dc voltage source points from the positive "+" lead to the negative "-" lead of that source. Finally, we assign arbitrary directions to all edges corresponding to current flowing through the resistors.

We choose a special enumeration scheme for the edges of our circuit. First we count and label all edges corresponding to resistors as edges $e_1, e_2, ..., e_{m_r}$. We continue our edge count by labeling the edges associated with the voltage sources, yielding edges $e_{m_r+1}, ..., e_{m_r+m_v}$. Finally, we enumerate our edges corresponding to current sources, producing edges $e_{m_r+m_v+1}, ..., e_m$. The only condition required in each count is that we have a bijection between circuit elements and graph edges. Although no specific sub-ordering is necessary, we recommend counting from top to bottom, left to right whenever possible.

By enumerating our edges using these guidelines, we enable a useful partition of the matrices and vectors that model our circuit. Figure 3 below combines our rules for drawing directed edges with the enumeration scheme to produce a visual representation of the digraph model for our electric circuit from Figure 1. If we want to write our choice of edges in set notation, we state that

$$\mathcal{E} = \{\underbrace{(1,7)}_{e_1}, \underbrace{(2,1)}_{e_2}, \underbrace{(2,7)}_{e_3}, \underbrace{(2,3)}_{e_4}, \underbrace{(3,6)}_{e_5}, \underbrace{(6,7)}_{e_6}, \underbrace{(3,4)}_{e_7}, \underbrace{(5,6)}_{e_8}, \underbrace{(2,7)}_{e_9}, \underbrace{(4,5)}_{e_{10}}, \underbrace{(4,2)}_{e_{11}}, \underbrace{(7,5)}_{e_{12}}\}.$$

Step 2C: Draw a directed graph model of the circuit.

Using the guidelines provided above, we draw a digraph model of our circuit, seen in Figure 3.



Figure 3: A digraph model for the example circuit in Figure 1 with ideal circuit elements replaced by directed edges using the enumeration and direction conventions described in step 2B above.

Step 3: Create all circuit matrices

In step three of the LANA algorithm we create all matrices used to model the behavior of our circuit. These include the entire incidence matrix A_g , the vector of node voltage potentials \mathbf{u}_g , the voltage-drop vector \mathbf{v} , and the current vector \mathbf{i} .

Step 3A: Create the entire incidence matrix

The entire incidence matrix captures the connectivity of the nodes in directed graph model of the circuit. The entry-by-entry definition of the entire incidence matrix $A_g \in \mathbb{R}^{m \times n_g}$ is given by

$$a_{jk} = \begin{cases} 1 & \text{if edge } e_j \text{ leaves node } k, \\ -1 & \text{if edge } e_j \text{ enters node } k, \\ 0 & \text{otherwise,} \end{cases}$$

for j = 1, 2, ..., m and $k = 1, 2, ..., n_g$. We see that the rows and columns of this matrix correspond to the edges and the nodes of our digraph, respectively. Below we set up this entire incidence matrix including our desired subblock partitions based on element type:

$$A_{g} = \begin{bmatrix} & & \\$$

where $A_{r_g} \in \mathbb{R}^{m_r \times n_g}$, $A_{v_g} \in \mathbb{R}^{m_v \times n_g}$, and $A_{i_g} \in \mathbb{R}^{m_i \times n_g}$. When defining the block partitions of any matrix or vector in our modeling scheme, we us subscripts r, v, and i denote the subblocks corresponding to digraph edges that encode resistors, voltage sources, and current sources, respectively.

Step 3B: Create the node voltage potential vector

From step 1 of our algorithm, we know this there are $n_g = 7$ distinct nodes in this circuit. We create a vector $\mathbf{u}_g \in \mathbb{R}^{n_g}$ of node voltage potentials given by

	u_1		the voltage potential of node 1
	u_2		the voltage potential of node 2
	u_3		the voltage potential of node 3
$\mathbf{u}_a =$	u_4	=	the voltage potential of node 4
3	u_5		the voltage potential of node 5
	u_6		the voltage potential of node 6
	u_7		the voltage potential of node 7

As described below in step 6 of the LANA algorithm, we designate a *datum node* $d \in \mathcal{N}$, also called the *ground node*, and set the corresponding voltage potential $u_d = 0$. However, in this early stage of our modeling process, we include all node voltage potentials in the vector \mathbf{u}_g . The subscript g means that the ground node voltage potential is still included in the model and has yet to be set to zero.

Step 3C: Create the voltage drop vector

Next, we create vector $\mathbf{v} \in \mathbb{R}^m$ that stores the voltage drop across each element, with

	\mathbf{v}_r		v_1		the voltage drop across resistor 1
			v_2		the voltage drop across resistor 2
			v_3		the voltage drop across resistor 3
			v_4		the voltage drop across resistor 4
			v_5		the voltage drop across resistor 5
			v_6		the voltage drop across resistor 6
$\mathbf{v} =$			v_7	=	the voltage drop across resistor 7
			v_8		the voltage drop across resistor 8
			v_9		the voltage drop across voltage source 1
	\mathbf{v}_v		v_{10}		the voltage drop across voltage source 2
			v_{11}		the voltage drop across current source 1
	\mathbf{v}_i		v_{12}		the voltage drop across current source 2

where $\mathbf{v}_r \in \mathbb{R}^{m_r}$, $\mathbf{v}_v \in \mathbb{R}^{m_v}$, and $\mathbf{v}_i \in \mathbb{R}^{m_i}$. Since we calculate one voltage drop across each element and there are precisely m = 12 elements in our circuit, we know there are exactly 12 entries in this vector. Due to our chosen strategy for enumerating the edges, the vector \mathbf{v} lists all voltage drops across the resistors followed by the voltage drops across the voltage sources and ending with voltage drops across the current sources. The stated partition of \mathbf{v} includes subblocks $\mathbf{v}_r, \mathbf{v}_v, \mathbf{v}_i$ that follow from this ordering.

Step 3D: Create the current vector

Finally, we create vector $\mathbf{i} \in \mathbb{R}^m$ to store the current running through each element, given by

i = [i		=	$egin{array}{ccc} i_1 & \hline i_2 & \\ i_3 & \hline i_3 & \end{array}$	$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \\ i_7 \\ i_8 \\ \vdots \\ i_9 \\ i_{10} \end{bmatrix} =$	the current through resistor 1 the current through resistor 2 the current through resistor 3
	\mathbf{i}_r		$egin{array}{c} i_4 \ i_5 \ i_6 \ i_7 \end{array}$		the current through resistor 4 the current through resistor 5 the current through resistor 6 the current through resistor 7
	\mathbf{i}_v		$egin{array}{c} i_8 \ i_{9} \ i_{10} \end{array}$		the current through resistor 8 the current through voltage source 1 the current through voltage source 2
	\mathbf{i}_i		$egin{array}{c} i_{11} \ i_{12} \end{array}$		the current through current source 1 the current through current source 2

where $\mathbf{i}_r \in \mathbb{R}^{m_r}$, $\mathbf{i}_v \in \mathbb{R}^{m_v}$, and $\mathbf{i}_i \in \mathbb{R}^{m_i}$. Since we calculate one current through each element in our circuit and since there are precisely 12 branches in this example network, we know there are exactly 12 entries in this vector. Again, using the same convention, we list all currents through the resistors first, followed by the currents through the voltage sources, and finally the currents through the current sources.

A count of variables

Notice that not all the scalar entries of the vectors $\mathbf{v}, \mathbf{i} \in \mathbb{R}^m$ are unknown variables. Specifically, the vectors \mathbf{v}_v and \mathbf{i}_i store known constants defined by the voltage and current levels provided by the independent sources we use to power our physical circuit. In this example, the assigned values for each dc voltage source in Figure 1 indicate that

$$\mathbf{v}_{v} = \begin{bmatrix} v_{v_1} \\ v_{v_2} \end{bmatrix} = \begin{bmatrix} v_9 \\ v_{10} \end{bmatrix} = \begin{bmatrix} 5 \\ 5 \end{bmatrix}.$$

For $j = 1, ..., m_v$, we say that v_{v_j} represents the assigned voltage value of the *j*th dc voltage source Vj in our circuit, where these constants are measured in volts. Using the same reasoning, we know that

$$\mathbf{i}_i = \begin{bmatrix} i_{i_1} \\ i_{i_2} \end{bmatrix} = \begin{bmatrix} i_{11} \\ i_{12} \end{bmatrix} = \begin{bmatrix} 2.5 \\ 2.5 \end{bmatrix}.$$

For $j = 1, ..., m_i$, we say that i_{ij} represents the assigned current running through the *j*th dc current source Ij in our circuit, as measured in milliamps.

To completely analyze the circuit at this point, the number of unknown variables remaining is

$$\ell = 2 \ m_r + m_v + m_i + n_q.$$

Directly solving a system involving this many unknowns is computationally expensive. Thus, in steps 4-6 of the LANA algorithm, we simplify our analysis problem by imposing constraints amongst the ℓ unknowns to produce a minimal set of n variables from which all other values can be calculated. For the circuit in Figure 1, this yields a reduction from $\ell = 27$ to n = 4 variables.

Optional Extension to Step 3: Label all variables and reference directions

One unnecessary but illuminating is to redraw the ideal circuit model and explicitly label unknown variables for every circuit element, as seen in Figure 4 below. This includes reference directions for the voltage drop across and the current running through each element. Notice that these reference directions follow the conventions outlined in step 2B above and also conform to the *passive sign convention* in which the current arrow points from positive to negative.



Figure 4: Redrawn Ideal Circuit Schematic Diagram with all variables labeled.

Step 4: State the entire set of circuit equations

The fourth step of the LANA algorithm is to state the entire set of circuit equations which come from Kirchhoff's current laws (KCLs), branch constitutive relations (BCRs), and Kirchhoff's voltage laws (KVLs). By combining these equations together, we achieve the first of two different reductions processes that eventually result in our minimal set of unknown circuit variables.

Step 4A: State the entire set of Kirchoff's current laws (KCLs)

We crafting our circuit equations by stating the *entire set of KCLs* as

$$A_g^T \mathbf{i} = \mathbf{0} \qquad \Leftrightarrow \qquad \left[\begin{array}{c} A_{r_g}^T \mid A_{v_g}^T \mid A_{i_g}^T \end{array} \right] \begin{bmatrix} \mathbf{i}_r \\ \mathbf{i}_v \\ \mathbf{i}_i \end{bmatrix} = \mathbf{0} \qquad (1)$$

Since both A_q and **i** are block partitioned matrices, we can restate our KCL's as

$$A_{r_g}^T \cdot \mathbf{i}_r + A_{v_g}^T \cdot \mathbf{i}_v + A_{i_g}^T \cdot \mathbf{i}_i = \mathbf{0}$$

The vector \mathbf{i}_i is a known and we bring this term on the right-hand side yielding

$$A_{r_a}^T \mathbf{i}_r + A_{v_a}^T \mathbf{i}_v = -A_{i_a}^T \mathbf{i}_i, \tag{2}$$

where \mathbf{i}_r and \mathbf{i}_v are two unknown quantities to be reduced. The entry-by-entry form of our KCLs is given by

$$\begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \\ -1 & 0 & -1 & 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \\ i_7 \\ i_8 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 1 & 0 \\ 0 & -1 \\ 0 & -1 \\ 0 & -1 \\ 0 & -1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_9 \\ i_{10} \end{bmatrix} = -\begin{bmatrix} 0 & 0 \\ -1 & 0 \\ 0 & 0 \\ 1 & 0 \\ 0 & -1 \\ 0 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{11} \\ i_{12} \end{bmatrix}$$

Recall that for the entire incidence matrix A_g , each column corresponds to the nodes of our circuit while the rows correspond to the circuit elements. The KCL equations are written using the transpose of A_g which swaps rows and columns. Thus, each row of the KCL matrix equation (1) encodes the sum of all currents that enter and leave the corresponding node.

Step 5B: State the branch constituent relations (BCRs)

To eliminate explicit reference to the \mathbf{i}_r vector in the matrix KCL equation (2), we use *branch constitutive relations* (BCRs). For resistive networks, the BCRs come in the form of *Ohm's law* which describes a linear relationship between the current flowing through and the voltage drop across a resistor. We capture this information for all resistors in the circuit using a matrix equation via either the *resistance* or *conductance* form given by

$$\mathbf{v}_r = R \,\mathbf{i}_r \qquad \qquad \text{or} \qquad \qquad \mathbf{i}_r = G \,\mathbf{v}_r. \tag{3}$$

The resistance matrix $R \in \mathbb{R}^{m_r \times m_r}$ is a diagonal matrix with the appropriate resistance values in each diagonal entry so that $v_k = r_k i_k$ for $k = 1, 2, ..., m_r$. The kth resistor Rk has positive resistance value $r_k > 0$ and we can rewrite Ohm's law equations in conductance form, where the conductance matrix $G = R^{-1}$ is a diagonal and the main diagonal entries are defined by the conductances $g_k = 1/r_k$.

In our example circuit, we have

$$\mathbf{i}_{r} = G \, \mathbf{v}_{r} \qquad \Leftrightarrow \qquad \begin{bmatrix} i_{1} \\ i_{2} \\ i_{3} \\ i_{4} \\ i_{5} \\ i_{6} \\ i_{7} \\ i_{8} \end{bmatrix} = \begin{bmatrix} g_{1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & g_{2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & g_{3} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & g_{4} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & g_{5} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & g_{6} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & g_{7} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & g_{8} \end{bmatrix} \begin{bmatrix} v_{1} \\ v_{2} \\ v_{3} \\ v_{4} \\ v_{5} \\ v_{6} \\ v_{7} \\ v_{8} \end{bmatrix}$$
(4)

Since we want to replace \mathbf{i}_r in the sublock KCL equations (2), we rely on the conductance form involving matrix G. This yields the partially reduced equation

$$A_{r_g}^T G \mathbf{v}_r + A_{v_g}^T \mathbf{i}_v = -A_{i_g}^T \mathbf{i}_i.$$
(5)

From here, we further simplify our work by identifying the relationship between the voltage drop vector \mathbf{v}_r and node potential vector \mathbf{u}_q .

Step 4C: State the entire set of Kirchoff's voltage laws (KVLs)

To connect the voltage drop and node potential variables, we use *Kirchhoff's voltage laws (KVLs) in node potential form*. These equations state that the voltage drop across each two-terminal element is calculated by the difference between the node voltage potentials at each terminal. Because the topology of our circuit is encoded in the entire incidence matrix A_q , we write the KVLs in matrix form as

$$A_g \mathbf{u}_g = \mathbf{v} \qquad \Leftrightarrow \qquad \qquad \left[\begin{array}{c} A_{r_g} \mathbf{u}_g \\ A_{v_g} \mathbf{u}_g \\ A_{i_g} \mathbf{u}_g \end{array} \right] = \left[\begin{array}{c} \mathbf{v}_r \\ \mathbf{v}_v \\ \mathbf{v}_i \end{array} \right]$$

Using the subblock partitions of the incidence matrix A_g and voltage drop vector \mathbf{v} , we state the *element-specific KVLs*. We begin with the *entire set of resistor KVLs* given by

$$A_{r_g} \mathbf{u}_g = \mathbf{v}_r \qquad \Leftrightarrow \qquad \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & -1 \\ -1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \\ u_6 \\ u_7 \end{bmatrix} = \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \\ v_7 \\ v_8 \end{bmatrix}$$
(6)

0

The second subblock equation is the *entire set of voltage source KVLs in node potential form* given by

$$A_{v_g} \mathbf{u}_g = \mathbf{v}_v \qquad \Leftrightarrow \qquad \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \\ u_6 \\ u_7 \end{bmatrix} = \begin{bmatrix} v_9 \\ v_{10} \end{bmatrix} = \begin{bmatrix} v_{v_1} \\ v_{v_2} \end{bmatrix}. \tag{7}$$

This equation is a general linear-systems problem with a known right-hand side. We return to this problem in steps 5 and 6 of our algorithm. Finally, the *entire set of current-source KVLs* are given by

$$A_{i_g} \mathbf{u}_g = \mathbf{v}_i \qquad \Leftrightarrow \qquad \begin{bmatrix} 0 & -1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 1 \end{bmatrix} \begin{vmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \\ u_6 \\ u_7 \end{vmatrix} = \begin{bmatrix} v_{11} \\ v_{12} \end{bmatrix}. \tag{8}$$

The matrix form of our KVL equations show that matrix-vector multiplication produces the values of \mathbf{v}_r and \mathbf{v}_i based on the entries of the vector \mathbf{u}_q .

Step 4D: Combine the circuit equations

Using the resistor KVLs (6), we replace vector \mathbf{v}_r in the partially reduced equation (5) with $A_{r_g} \mathbf{u}_g$ yielding

$$A_{r_g}^T G A_{r_g} \mathbf{u}_g + A_{v_g}^T \mathbf{i}_v = -A_{i_g}^T \mathbf{i}_i.$$
(9)

In producing this reduced system, we have two categories of data as shown in Table 1 below.

Known quantities	Unknown quantities
$A_{r_g}, A_{v_g}, A_{i_g}, G, \mathbf{v}_v, \mathbf{i}_i$	$\mathbf{u}_g,\mathbf{i}_v$

Table 1:	Known	and	unknown	quantities
----------	-------	-----	---------	------------

By combine the KCLs, BCRs, and KVLs together, we decrease the initial ℓ unknown variables to a smaller set of $(n_g + m_v)$ unknowns. For the circuit in Figure 1, this reduces $\ell = 27$ to $(n_g + m_v) = 9$ variables. We further reduce the number of variables needed to analyze the circuit by identifying constraints within the remaining unknown variables.

Step 5: Identify the ordinary and generalized nodes

Our next step is to determine the ordinary and generalized nodes of the circuit. We define an *ordinary node* of our system as a single circuit node to which no voltage source is connected. A *generalized node* in our system is a set of individual circuit nodes that are connected together by dc voltage sources.

To identify ordinary and generalized nodes, we use the *deactivated circuit heuristic* in which we deactivate the power sources by setting the value of each independent source to zero. This is equivalent to replacing each current source with an open circuit. Analogously, we replace each voltage source with a short circuit. When we apply this heuristic to the example circuit in Figure 1, we create the *deactivated resistor network* seen in Figure 4 below.



Figure 5: The deactivated resistor network for the example from Figure 1. Deactivation involves replacing each voltage source with a short circuit and each current source with an open circuit.

When we deactivate the circuit, a set of nodes that are linked via voltage sources meld together to form a single generalized node. Table 2 below presents these node classifications for the circuit in Figure 1.

Node Classification	Set of node indices	Node variables
Ordinary nodes	$\{1\},\{3\},\{6\}$	u_1, u_3, u_6
Generalized node 1	$\{4, 5\}$	u_4, u_5
Generalized node 2	$\{2,7\}$	u_2, u_7

Table 2: Classification of ordinary and generalized nodes

The deactivated circuit heuristic is useful not only to identify ordinary and generalized nodes but also to elucidate key connectivity features within the circuit. The process of deactivating each voltage source merges two nodes together thus eliminating m_v nodes from the original circuit. In contrast, deactivating the current sources does not change the number of nodes. What is left after the deactivation process is a circuit containing only resistors that are linked together via a reduced set of $(n_g - m_v)$ nodes.

Step 6: Create a minimal set of independent node potentials

The LANA algorithm uses linear algebra to reduce the vector \mathbf{u}_g to a minimal set of independent node variables from which all other quantities in the circuit can be calculated. To achieve this reduction, we partition the entries of \mathbf{u}_g into two lists. The first list of *constrained variables* includes one node potential variable for each voltage source and exactly one additional variable for our chosen ground node. The second list of *independent variables* are the chosen node voltage potentials that remain after eliminating the constrained quantities.

To impose the $(m_v + 1)$ constraints, we look at two features of our modeling problem. The first set of constraints is encoded in the voltage-source KVLs (7) which form a linear-systems problem since the vector \mathbf{v}_v on the right-hand side has known entries. This voltage source general linear-systems problem encodes m_v restrictions amongst the entries of \mathbf{u}_g . The second type of constraint relates to our choice of ground node. To ground our circuit, we pick a reference node and set one entry of the vector \mathbf{u}_g to zero. By partitioning the entries of \mathbf{u}_g in this way, we create a minimal list $\mathbf{u} \in \mathbb{R}^n$ of independent node variables, where $n = (n_g - m_v - 1)$. To reduce \mathbf{u}_g down to \mathbf{u} , we can first impose the voltage-source constraints and then choose a ground node from the remaining variables.

Step 6A: Impose one constraint for each voltage source

The voltage source KVLs (7) come in both matrix and scalar forms. For the example circuit in Figure 1, we use the matrix form to produce the scalar form with

$$A_{v_g} \mathbf{u}_g = \mathbf{v}_v \qquad \Leftrightarrow \qquad \begin{bmatrix} u_2 - u_7 \\ u_4 - u_5 \end{bmatrix} = \begin{bmatrix} v_{v_1} \\ v_{v_2} \end{bmatrix} = \begin{bmatrix} 5.0 \\ 5.0 \end{bmatrix} \tag{10}$$

We now search for a complete solution with $(n_g - m_v)$ free variables and m_v constraints. Since we have a choice of two different free variables for each voltage source, we have a total of $2 m_v$ different ways to produce a complete solution.

Let's look at one such choice for our example circuit. For the first generalized node, if we choose u_7 as the free variable, then $u_2 = u_7 + v_{v_1}$. For the second generalized node, if we choose u_4 as the free variable, then $u_5 = u_4 - v_{v_2}$. The resulting complete solution to the voltage-source KVLs (7) is

$$\begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \\ u_6 \\ u_7 \end{bmatrix} = \begin{bmatrix} u_1 \\ u_7 + v_{v_1} \\ u_4 \\ u_4 - v_{v_2} \\ u_6 \\ u_7 \end{bmatrix} = \begin{bmatrix} 0 \\ v_{v_1} \\ 0 \\ 0 \\ -v_{v_2} \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \underbrace{ \begin{bmatrix} u_1 \\ u_3 \\ u_4 \\ u_6 \\ u_7 \end{bmatrix} }_{\mathbf{u}_f}$$
(11)

No matter what choice we make for the free variables, we can always produce a complete solution to the voltage-source KVLs (7) in the form

$$\mathbf{u}_g = \mathbf{p}_g + Z_{v_g} \mathbf{u}_f \tag{12}$$

where $\mathbf{p}_g \in \mathbb{R}^{n_g}$ is a particular solution, the columns of $Z_{v_g} \in \mathbb{R}^{n_g \times n_f}$ form a basis for $\operatorname{Nul}(A_{v_g})$, the dimension $n_f = n_g - m_v$ represents the number of free variables from the voltage-source KVL equation (7), and $\mathbf{u}_f \in \mathbb{R}^{n_f}$ is the vector of free variables.

Step 6B: Impose one constraint for the ground node

To impose the final constraint and produce our minimal list of independent node potentials, we choose a single ground node from the remaining $(n_g - m_v)$ free variables. As described in step 6A above, let's assume that we chose free variables u_7 and u_4 for generalized nodes 1 and 2, respectively. This leaves five independent node potential variables which are u_1, u_3, u_4, u_6 and u_7 . We designate any of these remaining nodes as ground. The moment we choose ground, we shift the corresponding entry of the vector \mathbf{u}_f from unknown to known. This permits a dimension reduction realized using multiplication with a matrix $D_{f_0} \in \mathbb{R}^{n_f \times n}$ where

$$n = n_f - 1 = (n_g - m_v) - 1$$

is a nonnegative integer representing the minimum number of node voltage potentials needed to completely analyze the circuit. The form the matrix D_{f_0} , we take the $n_f \times n_f$ identity matrix and delete the column corresponding to our chosen ground node. For example, assume we ground node 7 and set $u_7 = 0$. We realize this constraint using the matrix equation

$$\underbrace{\begin{bmatrix} u_1\\ u_3\\ u_4\\ u_6 \end{bmatrix}}_{\mathbf{u}} = \underbrace{\begin{bmatrix} 1 & 0 & 0 & 0 & 0\\ 0 & 1 & 0 & 0 & 0\\ 0 & 0 & 1 & 0 & 0\\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ \end{bmatrix}}_{D_{f_0}^T} \underbrace{\begin{bmatrix} u_1\\ u_3\\ u_4\\ u_6\\ u_7 \end{bmatrix}}_{\mathbf{u}_f}$$

Notice that we have a choice of n_f different nodes that we can use as ground.

Step 6C: Combine the constraints together

We refer to this process of strategically deleting columns (or rows) of a matrix as *deflation*. Similarly, we say that a *deflation matrix* is any matrix used to delete or *deflate* the columns (or rows) of another matrix. No matter which node we ground, we use the deflation matrix D_{f_0} to define

$$\mathbf{u} = D_{f_0}^T \mathbf{u}_f \qquad \text{and} \qquad Z = Z_{v_a} D_{f_0}. \tag{13}$$

After grounding the circuit, we form a *completely reduced solution* to the voltage-source KVLs (7) given by

$$\mathbf{u}_g = \mathbf{p}_g + Z\mathbf{u} \tag{14}$$

where the columns of $Z \in \mathbb{R}^{n_g \times n}$ are in $\operatorname{Nul}(A_{v_g})$ and the vector $\mathbf{u} \in \mathbb{R}^n$ stores the minimal list of independent variables needed to fully analyze the circuit. This alternative form for the vector \mathbf{u}_g yields the desired equilibrium equation for our modeling problem. In this reduction, we define matrices

$$A_r = A_{r_q} Z, \qquad \qquad A_{v_q} Z = 0, \qquad \qquad \text{and} \qquad \qquad A_i = A_{i_q} Z. \tag{15}$$

Step 7A: State the equilibrium equation for the circuit

Looking back at our reduced system (9), we substitute \mathbf{u}_g with the completely reduced solution (14) and then multiply the entire equation (9) on the left-hand side by the matrix Z^T . This yields the matrix equation

$$A_r^T G A_r \mathbf{u} = A_r^T G \mathbf{b} - \mathbf{f},\tag{16}$$

where $\mathbf{b} = -A_{r_g} \mathbf{p}_g$ and $\mathbf{f} = A_i^T \mathbf{i}_i$. For almost any circuit that is used in real-world applications, the stiffness matrix $K = A_r^T G A_r$ is nonsingular.

Let's look more closely at the entry-by-entry definition of the stiffness matrix given as

The forcing terms on the right-hand side contain information about both the current sources and the effect of the voltage sources on the system. In particular, we notice that

$$\underbrace{\begin{bmatrix} 0\\0\\i_{i_1}-i_{i_2}\\\mathbf{f} \end{bmatrix}}_{\mathbf{f}} = \underbrace{\begin{bmatrix} 0&0\\0&0\\1&-1\\0&0\\A_i \end{bmatrix}}_{A_i} \underbrace{\begin{bmatrix} i_{i_1}\\i_{i_2}\\\mathbf{i}_i \end{bmatrix}}_{\mathbf{i}_i}$$

We also see that the voltage sources effect the system with

$$\begin{bmatrix} 0 \\ -v_{v_1} \\ -v_{v_1} \\ -v_{v_1} \\ 0 \\ 0 \\ 0 \\ v_{v_2} \end{bmatrix} = - \underbrace{ \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & -1 \\ -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \end{bmatrix} \underbrace{ \begin{bmatrix} 0 \\ v_{v_1} \\ 0 \\ 0 \\ -v_{v_2} \\ 0 \\ 0 \end{bmatrix} }_{\mathbf{P}_g}.$$

To calculate the resulting currents, we see that

Combining all of these results together, we produce the same system as espoused by the classical nodal analysis algorithm with

$$\underbrace{\begin{bmatrix} g_1 + g_2 & 0 & 0 & 0 \\ 0 & g_4 + g_5 + g_7 & -g_7 & -g_5 \\ 0 & -g_7 & g_7 + g_8 & -g_8 \\ 0 & -g_5 & -g_8 & g_5 + g_6 + g_8 \end{bmatrix}}_{K} \underbrace{\begin{bmatrix} u_1 \\ u_3 \\ u_4 \\ u_6 \end{bmatrix}}_{\mathbf{u}} = \underbrace{\begin{bmatrix} g_2 v_{v_1} \\ g_4 v_{v_1} \\ g_8 v_{v_2} \\ -g_8 v_{v_2} \end{bmatrix}}_{\mathbf{I}^T_r \mathbf{G} \mathbf{b}} - \underbrace{\begin{bmatrix} 0 \\ 0 \\ i_{11} - i_{12} \\ 0 \end{bmatrix}}_{\mathbf{f}}$$

© Jeffrey A. Anderson

We can transform this equation into numerical form by substituting the exact values for that circuit components designated in figure 1 yielding the system

$$\underbrace{\begin{bmatrix} 2 & 0 & 0 & 0 \\ 0 & 3 & -1 & -1 \\ 0 & -1 & 2 & -1 \\ 0 & -1 & -1 & 3 \end{bmatrix}}_{K} \underbrace{\begin{bmatrix} u_1 \\ u_3 \\ u_4 \\ u_6 \end{bmatrix}}_{\mathbf{u}} = \underbrace{\begin{bmatrix} 5 \\ 5 \\ -5 \\ -5 \end{bmatrix}}_{A_t^T G \mathbf{b} - \mathbf{f}}$$

Step 7B: Solve the equilibrium equation for the circuit

Now we solve our resulting 4×4 system using any method we'd like. Because the whole point of this exercise is to set ourselves up to take advantage of computer algorithms, let's use MATLAB to make this easier. On the companion website for this paper, readers can find a MATLAB script to solve this exact problem.

This example write up is dedicated to learners who may have relatively little coding experience. Thus, we include the entire solution process for completeness and ease of reference. We begin by transforming our matrix into upper-triangular form using Gauss transformations:

Using backward substitution, we see that

$$\mathbf{u} = \begin{bmatrix} u_1 \\ u_3 \\ u_4 \\ u_6 \end{bmatrix} = \begin{bmatrix} 2.50 \\ 3.75 \\ 5.00 \\ 1.25 \end{bmatrix}$$

We then substitute this result into the complete reduced solution (14) to see that

$$\begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \\ u_6 \\ u_7 \end{bmatrix} = \begin{bmatrix} 0 \\ v_{v_1} \\ 0 \\ 0 \\ -v_{v_2} \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \underbrace{ \begin{bmatrix} u_1 \\ u_3 \\ u_4 \\ u_6 \end{bmatrix}}_{\mathbf{u}} = \begin{bmatrix} 0 \\ 5 \\ 0 \\ 0 \\ -5 \\ 0 \\ 0 \end{bmatrix} + \underbrace{ \begin{bmatrix} 2.50 \\ 0.00 \\ 3.75 \\ 5.00 \\ 5.00 \\ 1.25 \\ 0.00 \end{bmatrix}}_{1.25} = \begin{bmatrix} 2.50 \\ 5.00 \\ 3.75 \\ 5.00 \\ 0.00 \\ 1.25 \\ 0.00 \end{bmatrix}$$

Step 7C: Calculate any desired circuit variable values

A very common problem in circuit analysis is to focus on a single circuit variable and find the value of that variable. One of the really cool features of the LANA algorithm is that, the moment we solve for our node voltage potential vector \mathbf{u}_g , we can find the value of any other circuit variable. For example, suppose we can use the resistor KVLs (6) to find the voltage drop across the resistors. Perhaps we want the current flowing through any resistor in the entire circuit. We can calculate these values using the the matrix version of Ohm's law equation in conductance form (3). The voltage drops across the current sources result from the current source KVLs (8). On the other hand, the currents running through the voltage sources pose a slightly more subtle problem. But we have is our KCL equation

$$A_{v_g}^T \cdot \mathbf{i}_v = -A_{r_g}^T G A_{r_g} \mathbf{u}_g - A_{i_g}^T \mathbf{i}_i.$$

The left-hand side includes two unknown variables while the right-hand side is completely determined by our previously stated constants.

Step 7D: Verify node voltage potentials in some other way(s)

Once we produce our ideal solution, we might want to verify our work using some alternate method. We might use a circuit simulation program like MultiSim or we might prototype the circuit using a solderless breadboard to take measurements using a digital multimeter. Table 3 below presents results from these alternative methods of verifying our modeled node voltage potential values.

Node	LANA model	MultiSim model	Physical measurement
Variable	values (V)	values (V)	values (V)
u_1	2.50	2.50	2.497
u_2	5.00	5.00	4.980
u_3	3.75	3.75	3.728
u_4	5.00	5.00	4.950
u_5	0.00	$-7.50 \mathrm{nV}$	0.003
u_6	1.25	1.25	1.241
u_7	0.00	0.00	0.000

Table 3: Model verification